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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/064,813

08/21/2002

Heng-Chien Chen

TRUP0002USA

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06/21/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)

P.O. BOX 506

MERRIFIELD, VA 22116

EXAMINER

GRIER, LAURA A

ART UNIT

PAPER NUMBER

2644

4

DATE MAILED: 06/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,813

Applicant(s)

CHEN, HENG-CHIEN

Examiner

Laura A Grier

Art Unit

2644

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claim 20** is rejected under 35 U.S.C. 102(e) as being anticipated by Shdema et al., Pub. No. 20020072816.

Regarding **claim 20**, Shdema et al. (herein, Shdema) discloses an audio system comprising wireless transmission of audio signals. Shdema disclosure includes a A/D converter for converting analog signals into digital signals (figures 1 – reference 106, and figure 3, reference 144, and page 5, paragraph 0051), wherein it is inherent that the A/D converter 144 comprise a plurality of A/D converters as evident by the fact that a plurality of audio sources are coupled the input of A/D converter 144, which reads on a plurality of A/D converters;

a transceiver (figure 1 – reference 110), which reads on a 1st transceiver;

computerized speaker (figure 1 – reference 114F and page 4, paragraph 0038) coupled to a wireless transceiver (112) indicating a wireless speaker module, and Shdema further discloses multiple wireless transceivers coupled to speakers (page 11, claim 3), which reads on a plurality of wireless speaker modules;

wireless transceiver (112) receives digital audio streams from wireless transceiver (110) – figures 1 and 3, which reads on a 2nd transceiver;

D/A converter for converting the digital signal to an analog signal (figure 4, reference 154A/B), a power amplifier array (164), which reads on an amplifier, and computerized speaker (114F), which reads on a speaker (page 6, paragraph 0066).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1-7, 11-18, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuqert et al, U. S. Patent No. 6466832 in view of Shdema et al.

Regarding **claim 1**, Zuqert et al. (herein, Zuqert) discloses a high quality wireless audio speakers (figures 1-2, and 10, col. 9, lines 10-23, and 67 - col. 10, lines 1-12). Zuqert's disclosure comprises a transmitter (22) of a wireless speaker system, which reads on a signal broadcasting circuit;

a multiplexer (52), for receiving a plurality of inputs (digital input, and left/right analog signals) and outputting an output, which reads on a multiplexer with a plurality of input nodes and on output node of a selected signal;

the transmitter (22) transmits digital signals to external speakers (44), and the transmitter may include a receiver as well (figure 10, 402- transmitting/receiving unit, and 404/406 –

speakers, col. 4, lines 59-64, and col. 20, lines 64-67 – col. 21, lines 1-2), which reads on a 1st transceiver for wireless transmitting the digital audio signals to external speakers;

the receivers (24/26) which include speakers (reference 44 and col. 9, lines 57-60, which reads on a plurality of wireless speaker modules,

and the receivers receives the digital signals from the transmitter (signal broadcasting circuit) and the receivers may include a transmitter as well (figure 10, 402-transmitting/receiving unit, and 404/406 – speakers, col. 4, lines 59-64, and col. 20, lines 64-67 – col. 21, lines 1-2), which reads on a 2nd transceiver;

a D/A converter (figure 7, reference 42), reads on a digital to analog converter;

and a speaker (44), which reads on a speaker.

Even though, Zuqert discloses an A/D converter (28), Zuqert fails to disclose an A/D converter receiving the selected output of the multiplexer. However, it would have been obvious to one of the ordinary skill in art to implement an A/D converter at the output of the multiplexer for digitizing an analog signal output by the multiplexer, wherein, it is a common technique for a multiplexer to process both analog and digital signals. And, further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an A/D converter at the output of multiplexer, since it has been held that rearranging parts of an invention involves only routing skill in the art. *In re Japikse*, 86 USPQ 70.

However, the Zuqert fails to disclose an amplifier for amplifying the analog audio for output the speaker.

Regarding the amplifier, Shdema et al. (herein, Shdema) discloses an audio system.

Shdema's disclosure comprises a power amplifier array (164) coupled to a computerized speaker (114F), which reads on an amplifier; which reads on an amplifier (page 6, paragraph 0066).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Zuqert by implementing a power amplifier after the D/A converter for the purpose of amplifying the signal to provide an enhanced quality sound output by the speaker.

5. Regarding **claim 11**, Zuqert discloses a high quality wireless audio speakers (figures 1-2, and 10, col. 9, lines 10-23, and 67 - col. 10, lines 1-12). Zuqert's disclosure comprises a transmitter (22) of a wireless speaker system, which reads on a signal broadcasting circuit;

a multiplexer (52), for receiving a plurality of inputs (digital input, and left/right analog signals) and outputting an output, which reads on a multiplexer with a plurality of input nodes and on output node of a selected signal;

the transmitter (22) transmits digital signals to external speakers (44), and the transmitter may include a receiver as well (figure 10, 402- transmitting/receiving unit, and 404/406 – speakers, col. 4, lines 59-64, and col. 20, lines 64-67 – col. 21, lines 1-2), which reads on a 1st transceiver for wireless transmitting the digital audio signals to external speakers;

the receivers (24/26) which include speakers (reference 44 and col. 9, lines 57-60, which reads on at least on wireless speaker modules,

the receivers (24/260 receives the digital signals from the transmitter (signal broadcasting circuit) and the receivers may include a transmitter as well (figure 10, 402-

transmitting/receiving unit, and 404/406 – speakers, col. 4, lines 59-64, and col. 20, lines 64-67 – col. 21, lines 1-2), which reads on a 2nd transceiver;

a D/A converter (figure 7, reference 42), reads on a digital to analog converter;
and a speaker (44), which reads on a speaker.

Even though, Zuqert discloses an A/D converter (28), Zuqert fails to disclose an A/D converter receiving the selected output of the multiplexer. However, it would have been obvious to one of the ordinary skill in art to implement an A/D converter at the output of the multiplexer for digitizing an analog signal output by the multiplexer, wherein, it is a common technique for a multiplexer to process both analog and digital signals. And, further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an A/D converter at the output of multiplexer, since it has been held that rearranging parts of an invention involves only routing skill in the art. *In re Japikse*, 86 USPQ 70.

Even though, Zuqert discloses a D/A converter, and speaker, Zuqert fails to disclose a plurality of amplifiers, a plurality of D/A converter, and plurality of speakers (herein, wireless speaker components) comprised in a one wireless speaker module.

Regarding the wireless speaker components, Shdema et al. (herein, Shdema) discloses an audio system including wireless speakers. Shdema's disclosure comprises D/A converter(s) for converting the digital signal to an analog signal (figure 4, reference 154A/B), reads on a plurality of D/A converters, a power amplifier array (164) including a plurality of amplifiers, each individually associated with a different frequency, which reads on a plurality of amplifiers; and plurality various speaker elements associated with a particular frequency (figure 4, references

166-172), which reads on a plurality of speakers (figure 1- 114F, page 4, paragraph 0038, page 6, paragraph 0066, and page 11, claim 3).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Zuqert by implementing the wireless speaker components for the purpose of adequately processing the audio signals to provide an enhanced and intelligent sound system as taught by Shdema.

Regarding **claim 2 and 12**, respectively, Zuqert and Shdema (herein, Zuqert combination) discloses everything claimed as applied above (see claim 1, and 11, respectively). Zuqert combination (Zuqert) discloses compressing and packaging the digital signals and associated preparations required of wireless digital transmission in the base-band processor (30) of the transmitter (signal broadcasting circuit) – col. 9, lines 25-36, which reads on the signal broadcasting circuit comprising a packaging and compressing circuit.

Regarding **claim 3 and 13**, Zuqert combination discloses everything claimed as applied above (see claim 2, and 12, respectively). Zuqert combination (Zuqert) discloses the processor (30) comprising a DSP, which is utilized in the compression and packaging process of the digital signals (col. 10, lines 13-26), which reads on the signal broadcasting circuit comprising a DSP.

Regarding **claim 4 and 14**, respectively, Zuqert combination discloses everything claimed as applied above (see claim 1, and 11, respectively). Zuqert combination (Zuqert) obviously discloses a sampling and control circuit as evident that the user interface is used for setting the multiplexer for determining which signal is selected via the A/D converter and the digital interface (col. 9, line 67 –col. 10, lines 1-7).

Regarding **claim 5 and 15**, Zuqert combination discloses everything claimed as applied above (see claim 1, and 11, respectively). Zuqert combination (Zuqert) discloses a processor (figure 7, reference 40), which is used in the operations of the receivers (24/26, speakers 44) – col. 9, lines 51-60, which reads on a processor for controlling the operation of the wireless speaker module.

Regarding **claim 6 and 16**, Zuqert combination discloses everything claimed as applied above (see claim 5, and 15, respectively). Zuqert combination (Zuqert) discloses the multiplexer choosing which signals are input to the processor for process, and processor assigns a pair of frequency channels (col. 10, lines 4-9, and col. 9, lines 38-40), wherein the multiplexer and processor coupled thereto reads on a channel selector, and processors of the receivers (speaker modules) process the signal accordingly, wherein the components of the receivers are compatible to the those of the transmitter (col. 12, lines 11-17, col. 16, lines 33-35).

Regarding **claim 7 and 17**, Zuqert combination discloses everything claimed as applied above (see claim 1, and 11, respectively). Zuqert combination (Zuqert) discloses a the processor (30/40) comprising a watchdog timer, which obviously indicates a diagnostic circuit as evident by the fact that the time resets the system upon any malfunctions (col. 10, lines 51-53).

Regarding **claim 8 and 18**, Zuqert combination discloses everything claimed as applied above (see claim 1, and 11, respectively). Zuqert combination (Zuqert) obviously disclose a timer for controlling the D/A convert as evident by the fact that the processor (40) includes a reset means (figure 7) and (watchdog timer – col. 10, lines 51-53) coupled to the system (logic and DSP), wherein the D/A converter is coupled thereto and controlled.

6. **Claims 9-10, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuqert combination in view of Kerr, SR., Pub. No. 20020152223.

Regarding **claim 9**, Zuqert combination discloses everything claimed as applied above (see claim 1). However, Zuqert combination fails to disclose the transmitted signal as direct sequence spread spectrum (DSSS) signals.

Regarding the DSSS signals, Kerr discloses a wireless connection between various communication devices, in which the wireless transmission or communication between the devices is implemented using DSSS environment (page 2, paragraph 0034, lines 9-12), which indicates DSSS signals.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Zuqert combination by using DSSS signal for the purpose of ensuring efficient transmission rates of the signals in a wireless network or environment in a home or office.

Regarding **claim 10**, Zuqert combination discloses everything claimed as applied above (see claim 1). Even though, Shdema disclose an IEEE protocol, the Zuqert combination fails to specifically disclose the system conforming to the IEEE 802.11b networking standard.

Regarding the IEEE 802.11b networking standard, Kerr, SR. (herein, Kerr) discloses a wireless connection between various communication devices, in which the wireless transmission or communication between the devices is implemented using the IEEE 802.11b networking standard (page 2, paragraph 0034, lines 1-5).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Zuqert combination by implementing the IEEE 802.11b

networking standard for the purpose of ensuring efficient and proper operation of the transmitter for transmitting the audio signals to wireless speakers.

Regarding **claim 19**, Zuqert combination discloses everything claimed as applied above (see claim 11). Claim 19 is interpreted as combination of claims 9 and 10, and thus rejected as indicated in the rejection of claims 9 and 10.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. **Claim 1** is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of copending Application No. 10064814. Although the conflicting claims are not identical, they are not patentably distinct from each other because each are drawn to the transmission of digital audio signals view transceivers to wireless speakers.

Regarding **claim 1**, Application No. 10064814 discloses in claim 20

a signal broadcasting circuit, which reads on a signal broadcasting circuit;

a 1st transceiver, which reads on a 1st transceiver;
a multiplexer, which reads on a multiplexer;
an analog to digital converter, which reads on an analog to digital converter;
a plurality of wireless speaker modules, which read on a plurality of wireless speaker modules;

a 2nd transceiver, which reads on a 2nd transceiver;
a digital to analog converter, which reads on a digital to analog converter,
an amplifier, which reads on an amplifier;
and a speaker, which reads on a speaker.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

12. Claims 11-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of copending Application No. 10064814 in view of Zuqert.

Regarding **claim 11**, Application No. 10064814 discloses in claim 11 a signal broadcasting circuit, which reads on a signal broadcasting circuit; a 1st transceiver which reads on a 1st transceiver; at least one multi-channel wireless speaker module which read on a multichannel wireless speaker module; a 2nd transceiver which reads on a 2nd transceiver; a plurality of digital to analog converters which reads on a plurality of digital to analog converters, an plurality of amplifiers which reads on a plurality of amplifiers; and a plurality of speakers which reads on a plurality of speakers.

Even though, Application No. 10064814 fails to disclose multiplexer and an A/D converter.

Regarding the multiplexer and an A/D converter, Zuqert discloses a multiplexer (52), for receiving a plurality of inputs (digital input, and left/right analog signals) and outputting an output, which reads on a multiplexer with a plurality of input nodes and on output node of a selected signal; and an A/D converter (28) . However, Zuqert fails to disclose an A/D converter receiving the selected output of the multiplexer. However, it would have been obvious to one of the ordinary skill in art to implement an A/D converter at the output of the multiplexer for digitizing an analog signal output by the multiplexer, wherein, it is a common technique for a multiplexer to process both analog and digital signals. And, further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an A/D converter at the output of multiplexer, since it has been held that rearranging parts of an invention involves only routing skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding **claim 12**, Application No. 10064814 discloses in claim 13 a packaging and compressing circuit which reads a packaging and compressing circuit.

Regarding **claim 14**, Application No. 10064814 discloses in claim 14 a sampling and control circuit which reads a sampling and control circuit.

Regarding **claim 15**, Application No. 10064814 discloses in claim 15 a processor, which reads on a processor.

Regarding **claim 16**, Application No. 10064814 discloses in claim 16 a channel selector, and a processor which reads on a channel selector and a processor.

Regarding **claim 17**, Application No. 10064814 discloses in claim 17 a diagnostic circuit which reads a on diagnostic circuit.

Regarding **claim 19**, Application No. 10064814 discloses in claim 18 direct sequence spread spectrum and IEEE 802.11b networking standard which reads direct sequence spread spectrum and IEEE 802.11b networking standard.

Regarding **claim 13**, Application No. 10064814 discloses everything claimed as applied above (see claim 12). However, Application No. 10064814 fails to disclose a DSP controlling the operation of the packaging and compressing circuit. Zuqert combination (Zuqert) discloses the processor (30) comprising a DSP, which is utilized in the compression and packaging process of the digital signals (col. 10, lines 13-26), which reads on the signal broadcasting circuit comprising a DSP.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Application No. 10064814 by implementing a DSP coupled to a processor for performing the compression and packaging of the audio signals and controlling the process for efficient digital audio transmission formatting for wireless transmission.

Regarding **claim 18**, Application No. 10064814 discloses everything claimed as applied above (see claim 11). However, Application No. 10064814 fails to disclose a timing circuit. Zuqert combination (Zuqert) obviously disclose a timer for controlling the D/A convert as evident by the fact that the processor (40) includes a reset means (figure 7) and (watchdog timer – col. 10, lines 51-53) coupled to the system (logic and DSP), wherein the D/A converter is coupled thereto and controlled.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Application No. 10064814 by implementing timing circuit (reset means) for the purpose of monitoring the operations of the system (D/A) converter for adequate processing the audio signals and resetting the system when a malfunction occurs for audio output.

This is a provisional obviousness-type double patenting rejection.

13. Claim 20 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of copending Application No. 10064814 in view of Shdema.

Regarding **claim 20**, Application No. 10064814 discloses in claim 20

a signal broadcasting circuit, which reads on a signal broadcasting circuit; a 1st transceiver which reads on a 1st transceiver; a multiplexer which reads on a multiplexer; a plurality of wireless speaker modules which read on a plurality of wireless speaker modules; a 2nd transceiver which reads on a 2nd transceiver; a digital to analog converter which reads on a digital to analog converter, an amplifier which reads on an amplifier; and a speaker which reads on a speaker. Even though, Application No. 10064814 disclose an analog to digital converter which reads on an analog to digital converter, Application No. 10064814 fails to disclose a plurality of A/D converters.

Regarding plurality of A/D converters, in similar field of endeavor, Shdema disclosure includes a A/D converter form converting analog signals into digital signals (figures 1 – reference 106, and figure 3, reference 144, and page 5, paragraph 0051), wherein it is inherent

Art Unit: 2644

that the A/D converter 144 comprise a plurality of A/D converters as evident by the fact that a plurality of audio sources are coupled the input of A/D converter 144, which reads on a plurality of A/D converters.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Application No. 10064814 by implementing a plurality of A/D converters for the purpose of converting a plurality of analog signals from analog audio sources into digital signals for adequate transmission through a wireless digital system.

This is a provisional obviousness-type double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura A Grier whose telephone number is (703) 306-4819. The examiner can normally be reached on Monday - Friday, 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Application/Control Number: 10/064,813

Page 16

Art Unit: 2644

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

LAG *Laura Alfrey*
June 14, 2004